FIG. 1

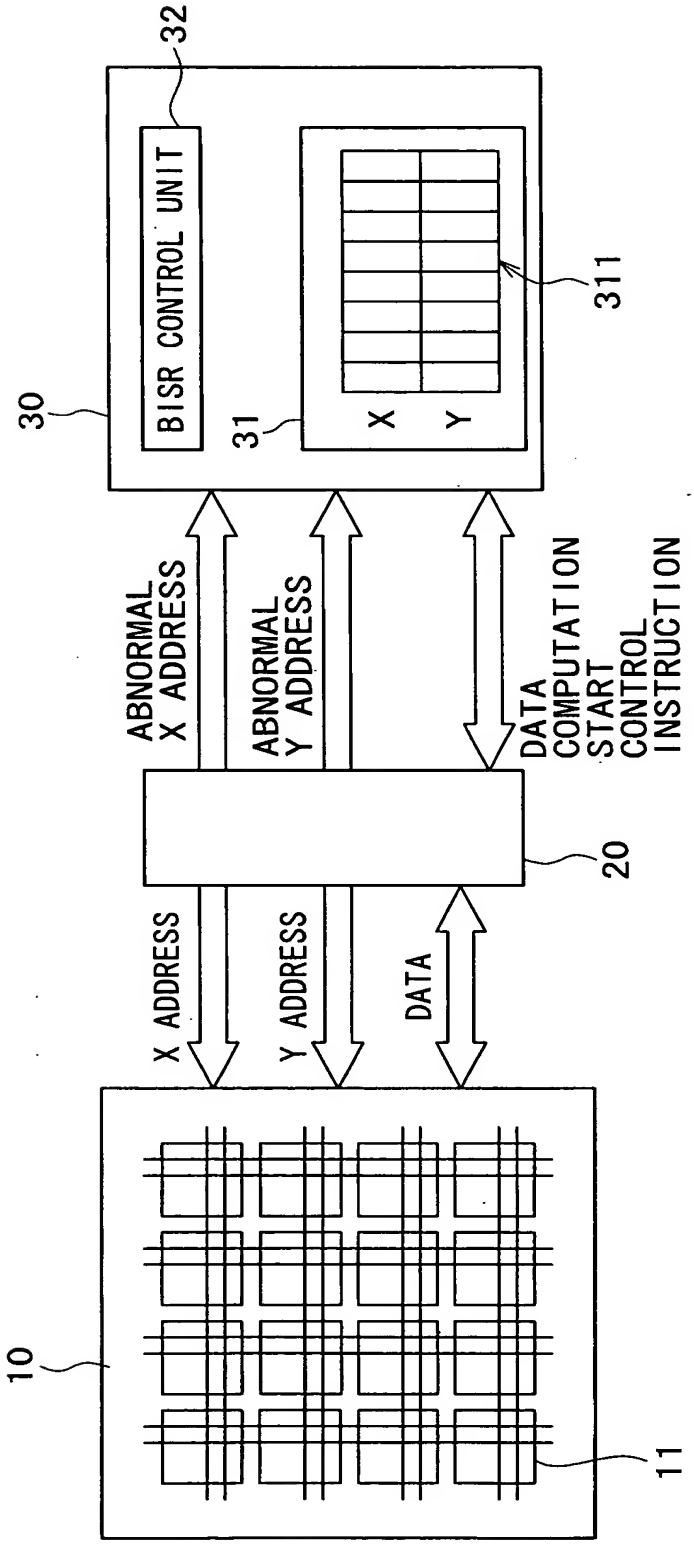
32
BISR CONTROL UNIT
30
31
311
X
Y
ABNORMAL X ADDRESS
ABNORMAL Y ADDRESS
DATA COMPUTATION START CONTROL INSTRUCTION
20
X ADDRESS
Y ADDRESS
DATA
10
11

FIG. 2

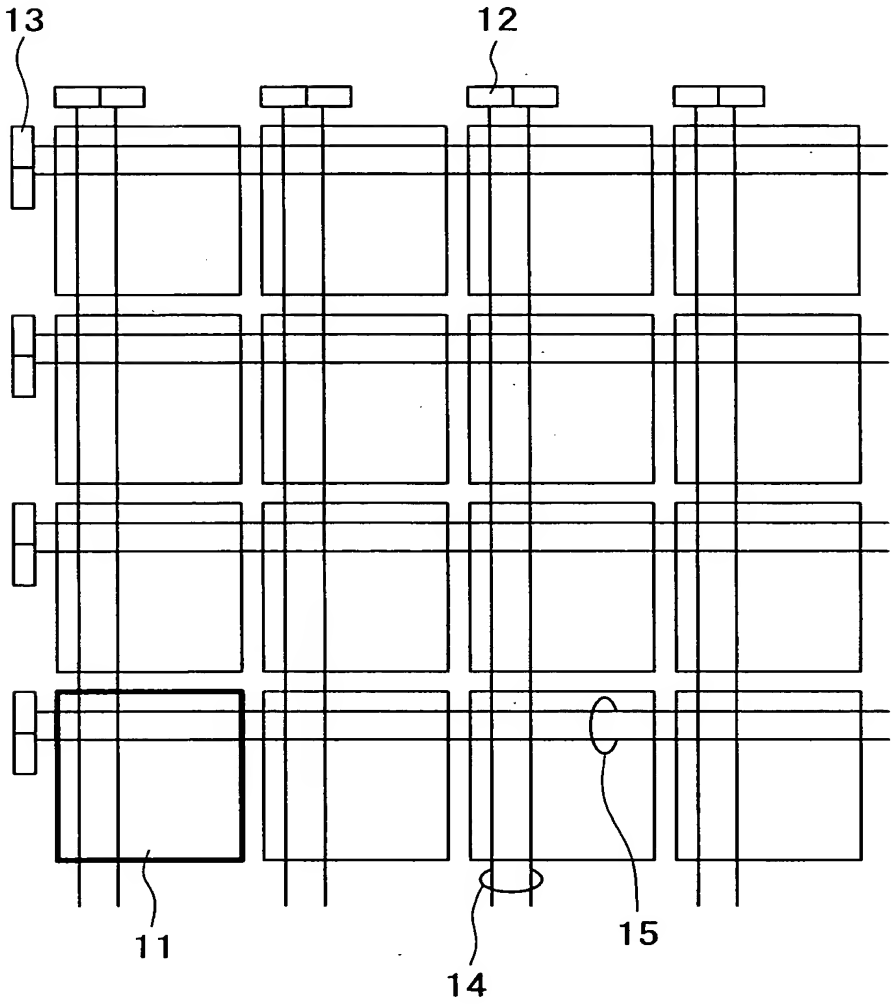

FIG. 3

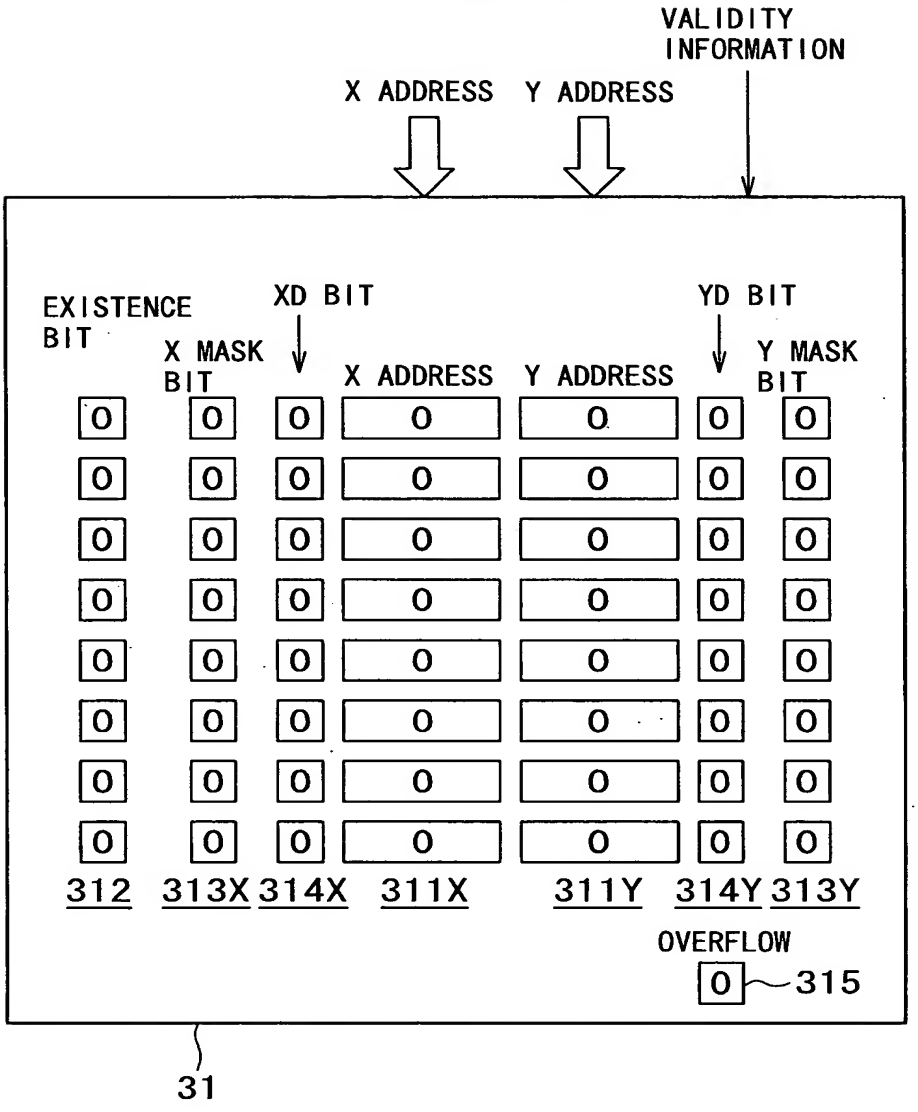
VALIDITY INFORMATION
X ADDRESS
Y ADDRESS
EXISTENCE BIT
XD BIT
YD BIT
X MASK BIT
X ADDRESS
Y ADDRESS
Y MASK BIT
0
312
313X
314X
311X
311Y
314Y
313Y
OVERFLOW
315
31

FIG. 4

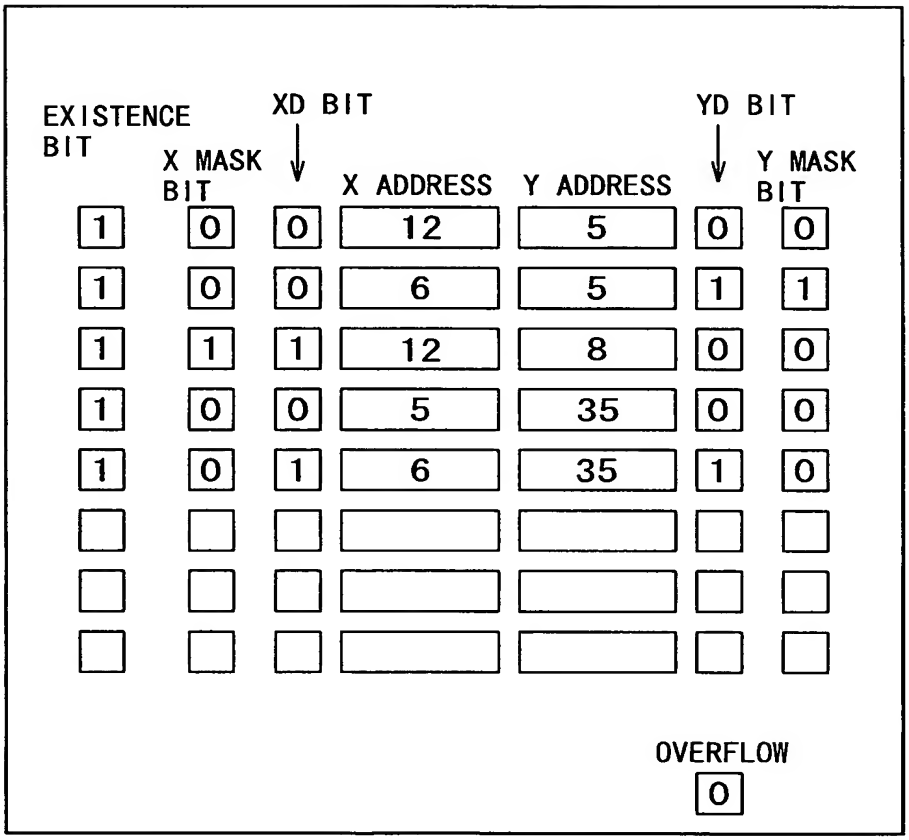
EXISTENCE BIT
X MASK BIT
XD BIT
X ADDRESS
Y ADDRESS
YD BIT
Y MASK BIT
1 0 0 12 5 0 0
1 0 0 6 5 1 1
1 1 1 12 8 0 0
1 0 0 5 35 0 0
1 0 1 6 35 1 0
OVERFLOW
0

FIG. 5

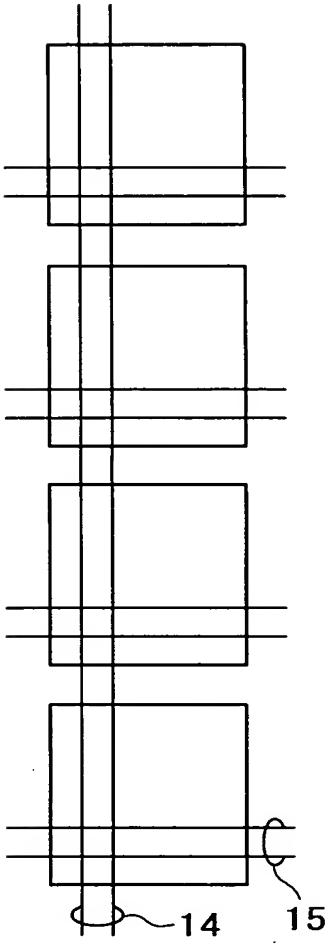

FIG. 6

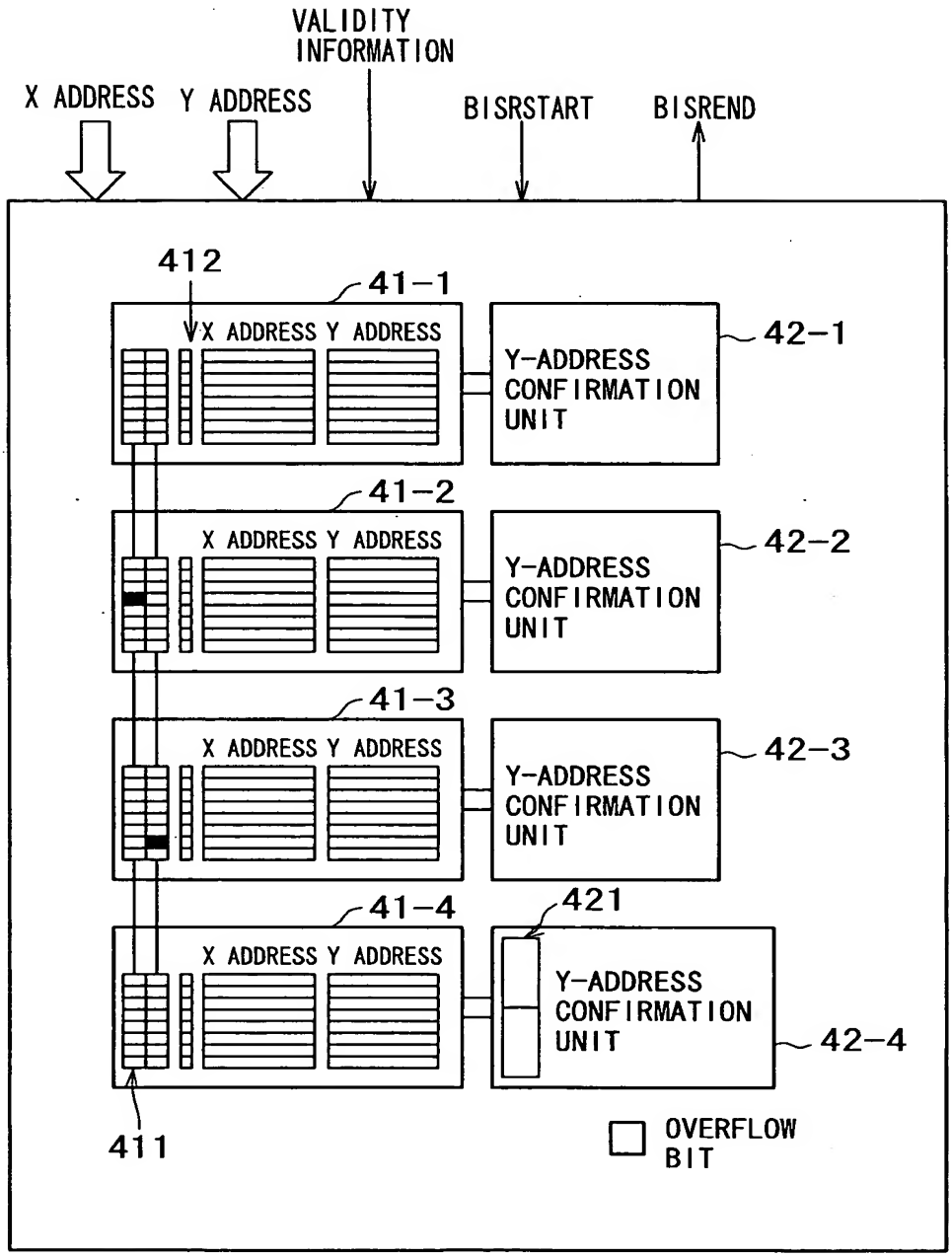
VALIDITY INFORMATION
X ADDRESS
Y ADDRESS
BISRSTART
BISREND
412
41-1
X ADDRESS Y ADDRESS
Y-ADDRESS CONFIRMATION UNIT
42-1
41-2
X ADDRESS Y ADDRESS
Y-ADDRESS CONFIRMATION UNIT
42-2
41-3
X ADDRESS Y ADDRESS
Y-ADDRESS CONFIRMATION UNIT
42-3
41-4
421
X ADDRESS Y ADDRESS
Y-ADDRESS CONFIRMATION UNIT
42-4
411
OVERFLOW BIT

FIG. 7

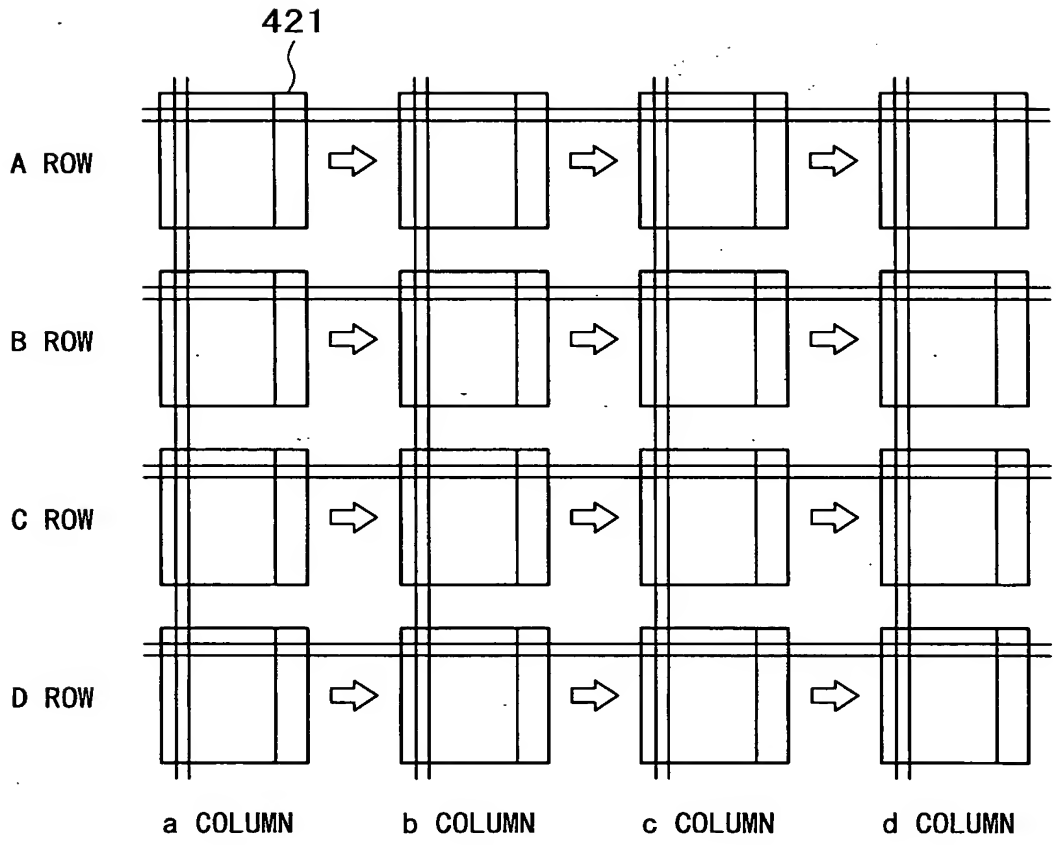

FIG. 8

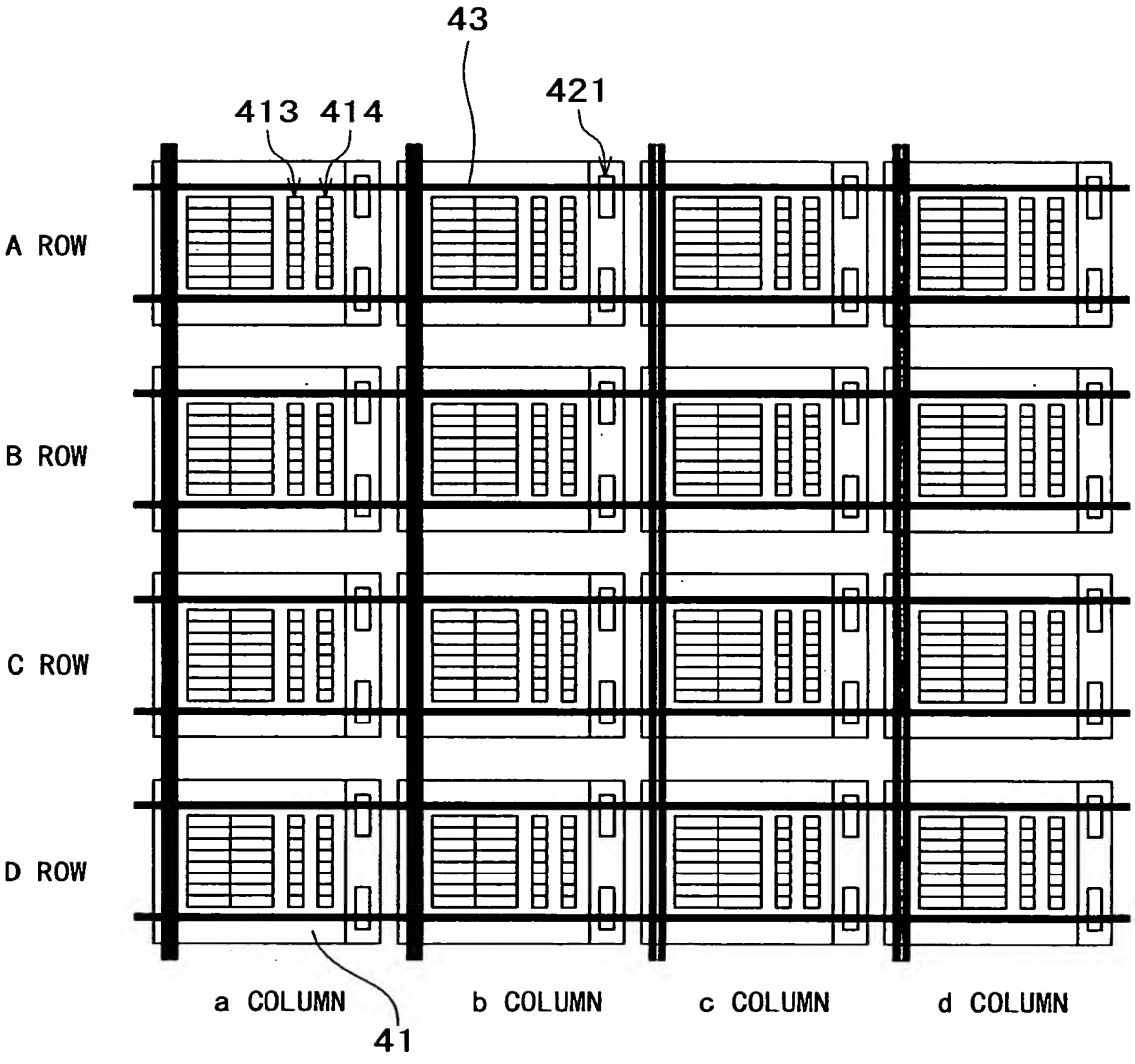
43
413
414
421
A ROW
B ROW
C ROW
D ROW
a COLUMN
b COLUMN
c COLUMN
d COLUMN
41

FIG. 9B

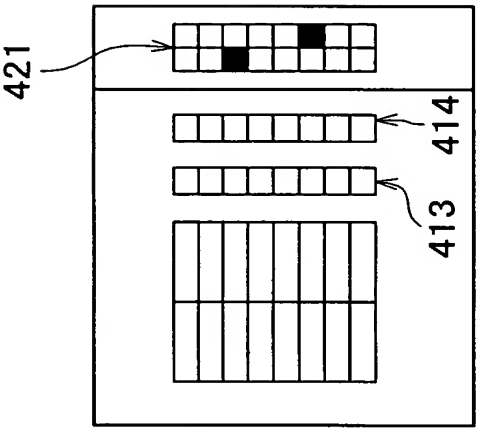

FIG. 9A

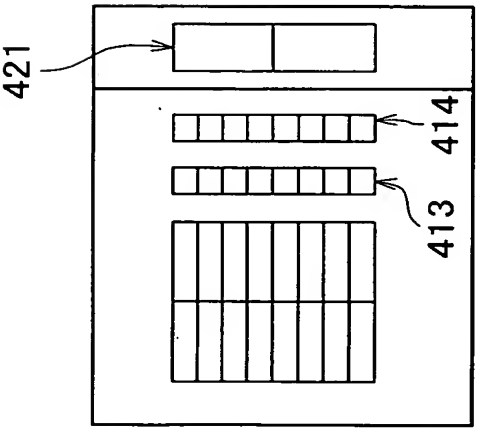

FIG. 10A

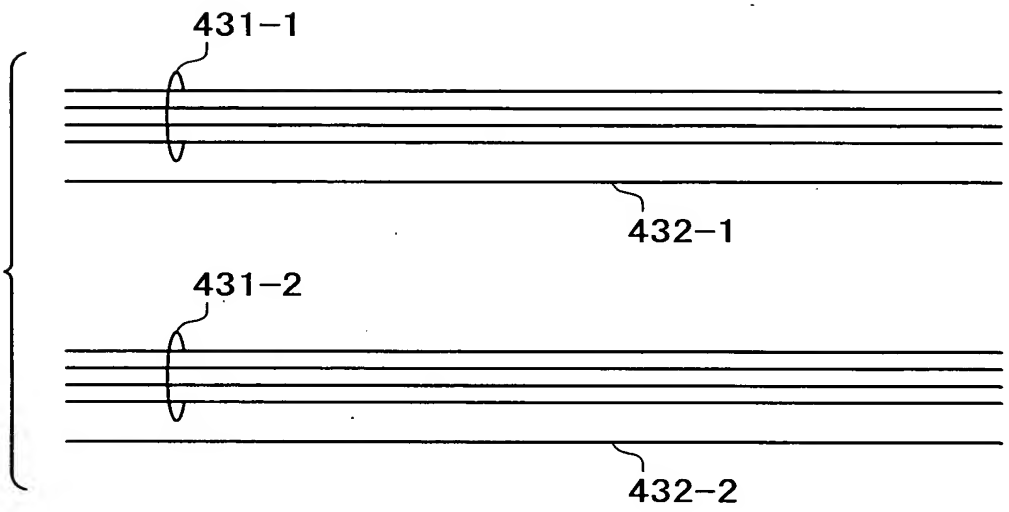

FIG. 10B